MULTILEVEL PARALLEL CRC GENERATION AND CHECKING CIRCUIT

ABSTRACT

A CRC generator/checker for generating CRC results, comprising: a set of CRC circuits connected in series, each CRC circuit responsive to a different control signal generated by a control logic, each CRC circuit having a seed input adapted to receive a seed, a data input adapted to receive and process a different set of M-bits of a data unit and a result output adapted to generate a result, the result output of a previous CRC circuit connected to the seed input of an immediately subsequent CRC circuit, the seed input of a first CRC circuit connected to an output of a remainder register, an input of the remainder register connected to an output of a multiplexer, the result outputs of the multiplicity of CRC circuits connected to different inputs of the multiplexer, the multiplexer responsive to a select signal generated by the control logic.